HIGH SPEED DIGITAL PHASE/FREQUENCY COMPARATOR FOR PHASE LOCKED LOOPS

Abstract of the Disclosure

An apparatus and method for detecting a phase difference between an input signal and a reference signal in an all-digital phase locked loop (PLL) are provided. In a preferred embodiment, an N-stage tapped delay line and N-bit parallel latch are used to create a snapshot of the the input signal by latching the output of the tapped delay line using the reference signal to clock the latch. An edge detector and encoder circuit translate the latched snapshot into a numerical phase difference value. A difference between this phase difference value and a desired phase difference is calculated and then added to an accumulator. The result in the accumulator is a numerical phase error value that can be fed to a numerically controlled oscillator (NCO). The output of the NCO can, in turn, be fed back into the phase/frequency comparator as the input signal, thus forming a fully-digital PLL.